

## GLOBAL JOURNAL OF ENGINEERING SCIENCE AND RESEARCHES EFFICIENT VLSI ARCHITECTURE FOR ADVANCED ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (AOFDM) SYSTEM FOR EFFICIENT COMMUNICATION

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### ABSTRACT

Most of the communication devices such as ADSL modem, digital audio/video broadcasting etc. needs a huge transmission rate which intern needs huge bandwidth. To overcome this bandwidth issues without affecting transmission rate Orthogonal Frequency Division Multiplexing (OFDM) technique is invented. Normally most OFDM trans-receivers are implemented using conventional analog components such as transistors, diodes, capacitors and resistors etc. which makes the whole encoding and decoding process bulky. Moreover the power consumption and total operating frequency is not in optimum level. As a result digital implementation of OFDM in single integrated circuits (ICs) came into picture. But most of the existing architectures are not very efficient in terms of hardware resources utilizations. In this paper, we propose novel hardware architecture to implement OFDM system using Field Programmable Gate Arrays (FPGAs). The total system is subdivided into two sections namely transmitter and receiver section. The comparison results shows that the proposed architecture is efficient than existing in various hardware aspects.

*Keywords: Orthogonal Frequency Division Multiplexing, FPGA Implementation, Transmitter, Receiver.*

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### I. INTRODUCTION

Basically, OFDM technique consists of dividing the flow of entrance knowledge over orthogonal channels. During this approach, and supported the orthogonality principle, the interference between every transmission is borderline. Another advantage that comes from this approach is expounded to the assumptions concerning the noise in every channel. Over an outsized and distinctive pass-band channel its tough (impossible after all, in several situations) to assume that the model noise is AWGN (Additive Noise Gaussian Noise). that's necessary as a result of if the model is apprehend, and it's correct, one will choose the most effective approach of frequency feat. But, in giant pass-band channels (tenths of MHz) the noise model is unknown and unpredictable. The answer of dividing a novel channel in sub-channels simplifies the assumptions of the noise over every sub-channel and, of course, one will suppose it about AWGN. In every one of those sub-channels, a digital modulation is formed, every one with a subcarrier that presents completely different frequency, in a very such kind that a channel doesn't intervene with another one, therefore keeping the orthogonality. The approach of implementation and therefore the orthogonality property of a system of this kind will vary sufficiently: since band pass filters every frequency till subtle techniques because the use of the FFT with guard interval, that is that the used one for the OFDM. This system has been drawn up some designations as orthogonally multiplexed QAM (O-QAM), parallel construction AM, and so one. However, OFDM for wireless and DMT for systems wired (like DSL) area unit the foremost common designations that one will notice

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in literature. As all the on top of techniques essentially use a similar principle, it's common to discuss with them by means that of a generic name: MCM (to Multi-Carrier Modulation). In this approach, MCM is that the technique within the general direction and OFDM is expounded to the implementation of technique MCM victimization the FFT.

## II. LITERATURE SURVEY

Yiyan Wu [1] presents a Multi-Carrier OFDM Scheme concentrating on various different design parameters like complexity, bandwidth, performance and flexibility. But the proposed design depicts some of the disadvantages where, since the peak-to-average power ratio is high, the transmitter output back off should be also high and since it is a multi-carrier scheme it has parallel transmission technique which increases the sensitivity of the OFDM system to the carrier frequency offset. AttaRahman [2] has designed the model in such a way that some of the parameters of OFDM system like power, code rate and modulation scheme are adapted as the conditions of channel varies in order to increase the throughput of the OFDM system using FRBS and GRBF-Neural Networks. Na-Na Huang [3] has published a novel idea which concentrates on the synchronization of underwater acoustic OFDM communication system designed based on fractional Fourier Transform (FRFT-OFDM) using new design Symmetrical Triangular Linear Frequency Modulation (STLFM) signal as preamble code. S.E.Alavi [4] has presented a novel design where the all-optical OFDM system uses MRR as filters and to generate very high frequency soliton signals. The system generates 64 optical carriers in order to setup the transmission system. 16-QAM is used to modulate the subcarriers and the OFDM generated is multiplexed with carrier soliton and transmitted through single-mode fiber and propagated through RF signal. Anand S. Bhosle [5] has discussed a valuable content presenting different tools and techniques for OFDM generation and optimization with respect to peak-to-average power ratio (PAPR). The author mentions some of the techniques clipping and filtering, partial transmit sequence, selective mapping, etc. and hardware tools FPGA, Cognitive Radio, etc. and software tools Matlab, LabView, Xilinx, etc. SandeepKaur [6] presents a review paper on wireless communication systems based on OFDM. The author discusses how the frequencies are selected in transmission channels and achieves a high data-rate with low ISI and how this is going to be used widespread in 4G communication systems. The author has compared the OFDM results with the other communication systems and concludes how OFDM is far better than them in digital audio broadcasting, digital video broadcasting, LAN, WiMax, etc. Praveen Pawar [7] has presented a review paper on the OFDM and PAPR where he explains the working of orthogonal frequency division multiplexing with encoding of the signal in multi carrier frequencies. He gives some of the advantages and disadvantages and also tells about some of the reduction techniques of the PAPR. Vishal Pasi [8] gives a brief summary of the orthogonal frequency division multiplexing (OFDM), its advantages and its applications. The author tells that OFDM is used because it is better than other wireless communication system with respect to PAPR, channel estimation and signal detection, intercarrier interference, multiple-input-multiple-output techniques. Sukhpal Singh [9] gives a review of the OFDM and some of the techniques used in it to increase the efficiency of the system. The author tells that OFDM is the source of the DSL standards and known as discrete multi-tone, where the sequential data is transformed into parallel stream. The IFFT is used to realize the computational and orthogonality concepts and analog filtering is required to de-multiplex the channels. Zakee Ahmed [10] discusses about some major PAPR reduction techniques in OFDM, where the reduction of PAPR is a very important parameter for the increasing of OFDM system efficiency. Some of the techniques discussed here are Amplitude Clipping and Filtering, Selected Mapping and Partial transmit sequence.

## III. BASICS OF OFDM

The structural synthesis of CCPGTs will be performed based on the creative design methodology process [7-8]. Fig.3 shows the flow chart for the approach. The process consists of six steps:

### 3.1 Transmitter

An OFDM carrier signal is that the total of variety of orthogonal sub-carriers, with baseband knowledge on every sub-carrier being severally modulated ordinarily victimization some sort of construction modulation (QAM) or phase-shift keying (PSK). This composite baseband signal is often accustomed modulate a main RF carrier.  $S[n]$  may be a serial stream of binary digits. By inverse multiplexing, these are initial de-multiplexed into  $N$  parallel streams, and every one mapped to (possibly complex) image stream victimization some modulation constellation

(QAM, PSK, etc.). Note that the constellations is also completely different, therefore some streams could carry thenext bit-rate than others. An inverse FFT is computed on every set of symbols, giving a collection of complicated time-domain samples. These samples are then quadrature mixed to pass-band within the normal method. The important and notional parts are initial regenerate to the analogue domain victimization digital-to-analogue converters (DACs); the analogue signals are then accustomed modulate trigonometric function and circular function waves at the carrier frequency,  $f_c$ , severally. These signals are then summed to present the transmission signal,  $s(t)$ .

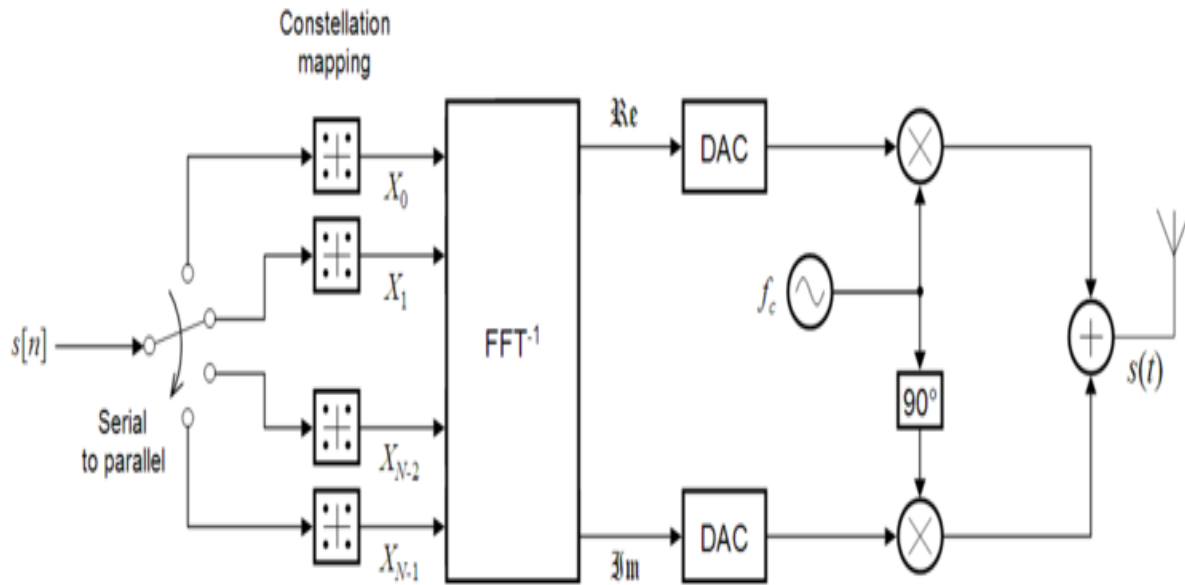


Fig.1. Transmitter Section of OFDM

### 3.2 Receiver

The receiver picks up the signal  $r(t)$ , that is then quadrature mixed right down to baseband victimization trigonometric function and sin waves at the carrier frequency. This conjointly creates signals targeted on  $2f_c$ , thus low-pass filters area unit wont to reject these. The baseband signals area unit then sampled and digitized victimization analog-to-digital converters (ADCs), and a forward FFT is employed to convert back to the frequency domain.

This returns  $N$  parallel streams, every of that is regenerate to binary stream victimization AN applicable image detector. These streams area unit then re-combined into a serial stream,  $s^{\wedge}(n)$ , that is AN estimate of the first binary stream at the transmitter.

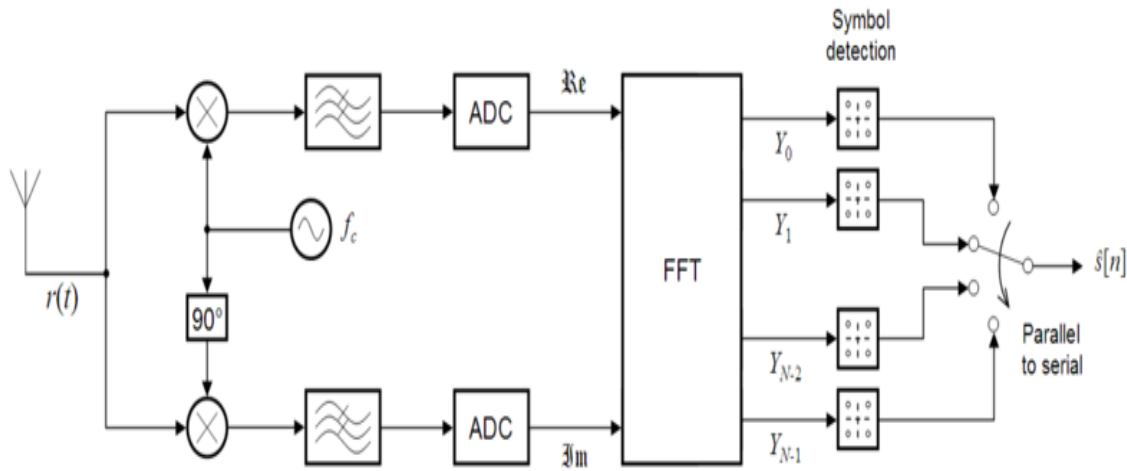


Fig.2. Receiver Section of OFDM

### 3.3 Mathematical Formulations

If N sub-carriers square measure used, and every sub-carrier is modulated mistreatment M various symbols, the OFDM image alphabet consists of MN combined symbols. The low-pass equivalent OFDM signal is expressed [11] as:

$$v(t) = \sum_{k=0}^{N-1} X_k e^{j\frac{2\pi kt}{T}}, \quad 0 \leq t < T(1)$$

Where  $X_k$  area unit the information symbols, N is that the variety of sub-carriers and T is that the OFDM image time. The sub-carrier spacing of  $1/T$  makes them orthogonal over every image period; this property is expressed [11] as

$$\frac{1}{T} \int_0^T e^{j\frac{2\pi(k_2-k_1)t}{T}} dt \quad (2)$$

To avoid inter-symbol interference in multipath attenuation channels, a guard interval of length  $T_g$  is inserted before the OFDM block. Throughout this interval, a cyclic prefix [11] is transmitted specified the signal within the interval  $-T_g \leq t$

$$v(t) = \sum_{k=0}^{N-1} X_k e^{j\frac{2\pi kt}{T}}, \quad -T_g \leq t < T \quad (3)$$

The low-pass signal on top of will be either real or complex-valued. Real-valued low-pass equivalent signals area unit usually transmitted at baseband—wire line applications corresponding to line use this approach. For wireless applications, the low-pass signal is usually complex-valued; within which case; the transmitted signal is up-converted to a carrier frequency  $f_c$ . In general, the transmitted signal will be described [11] as:

$$s(t) = \sum_{k=0}^{N-1} |X_k| \cos\left(2\pi\left[f_c + \frac{k}{T}\right]t + \arg\{X_k\}\right) \quad (4)$$

## IV. PROPOSED ARCHITECTURE

The proposed OFDM system is given in Fig.3. The total system is divided into two parts as transmitter and receiver part. The transmitter part [12] is used to convert the input data into suitable frequency division multiplexing format. In the transmitter part the serial data of a finite length is converted into the parallel format using “serial/parallel conversion” block whose outputs are encoded through “Encoder” block. The output of this block is in complex numbers which consists of many redundant components. The “Hermitian Symmetry” block is used to remove those redundancies to reduce total computation time. Now using “IFFT” and “Cyclic-Prefix” block the modulated datastream is sent serially over the communication channel.

At the receiver side the modulated data streams first synchronized to the receiver block for proper decoding by “Synchronization” block. The synchronized data is then converted to parallel format by “Parallel/Serial Conversion” block. Here the cyclic prefixes are eliminated which then fed to “FFT” block. In FFT the Hermitian Symmetry are cancelled which then converted block using a “Decoder” block. The decoder output is then converted into serial format which is the extracted data.

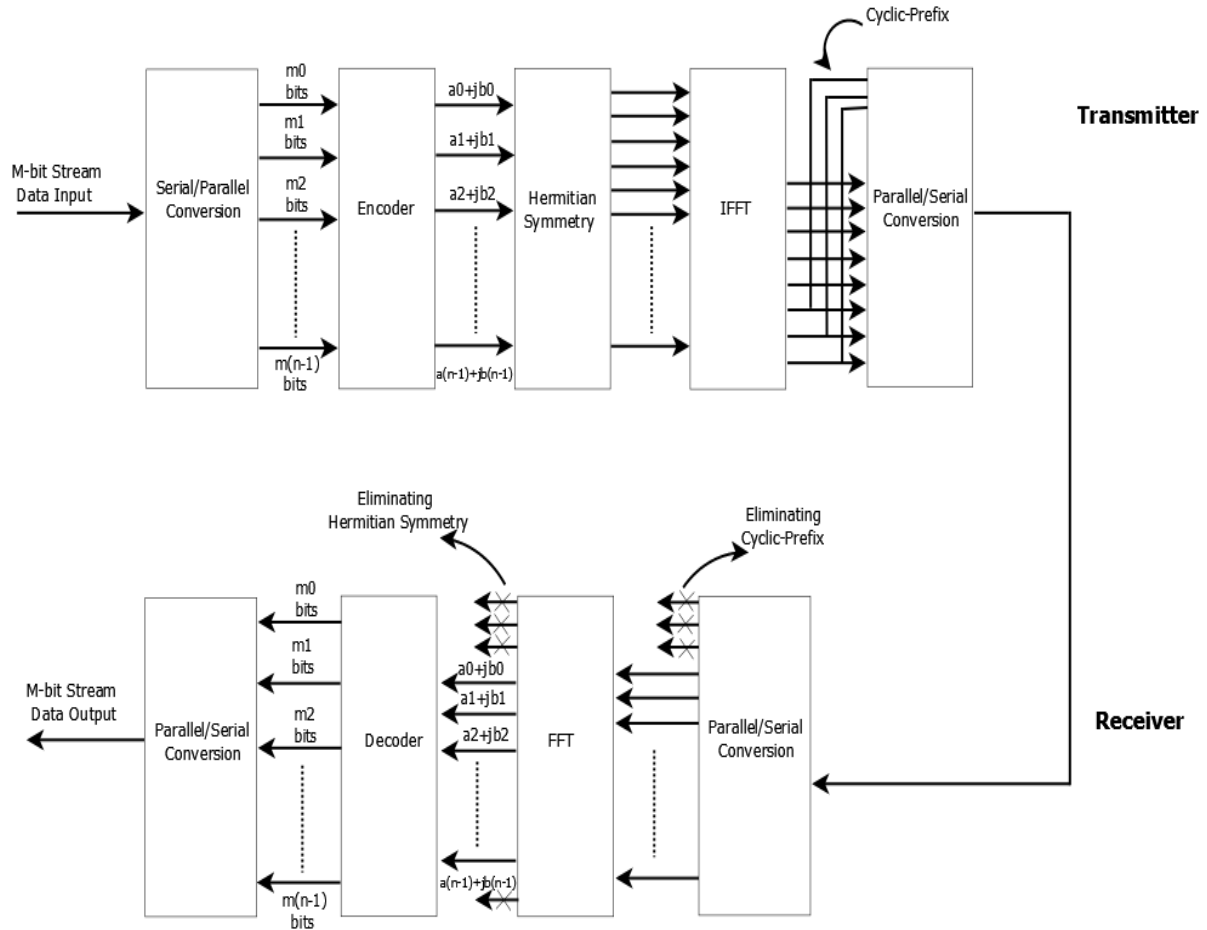


Fig.3. Proposed Architecture

**Transmitter part**

The transmitter part is used to convert the data stream into frequency division multiplex format. The architecture of the transmitter part [12] is given in Fig.4. It consists of data conversion, encoder, Hermitian Symmetry and IFFT.

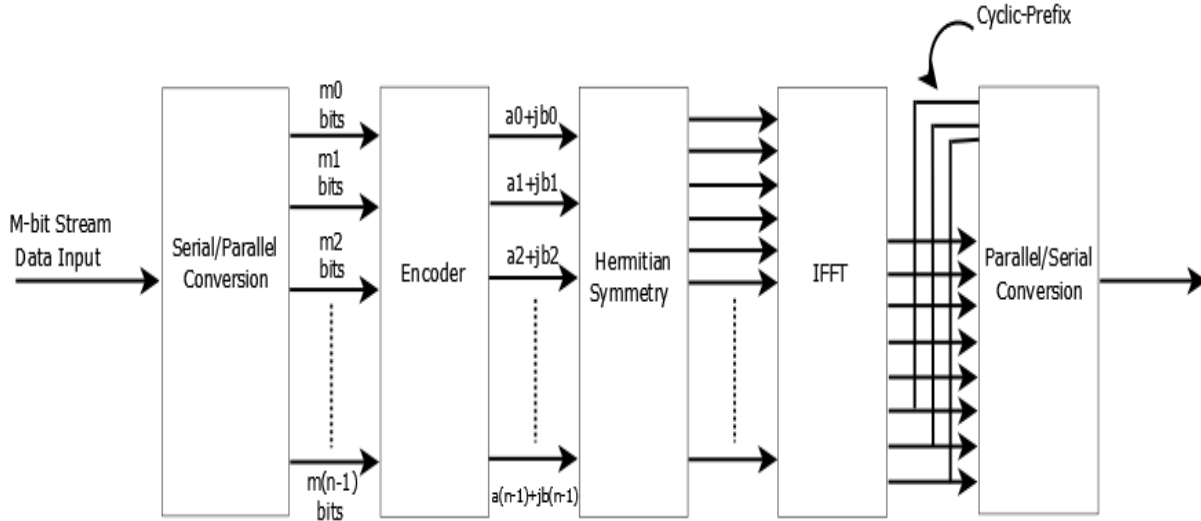


Fig.4. Transmitter Part

**Receiver part**

The Receiver part decrypts the modulated signal to generate the data stream which is equivalent to the input data stream of the transmitter part. The block diagram of the receiver is given in Fig.5.

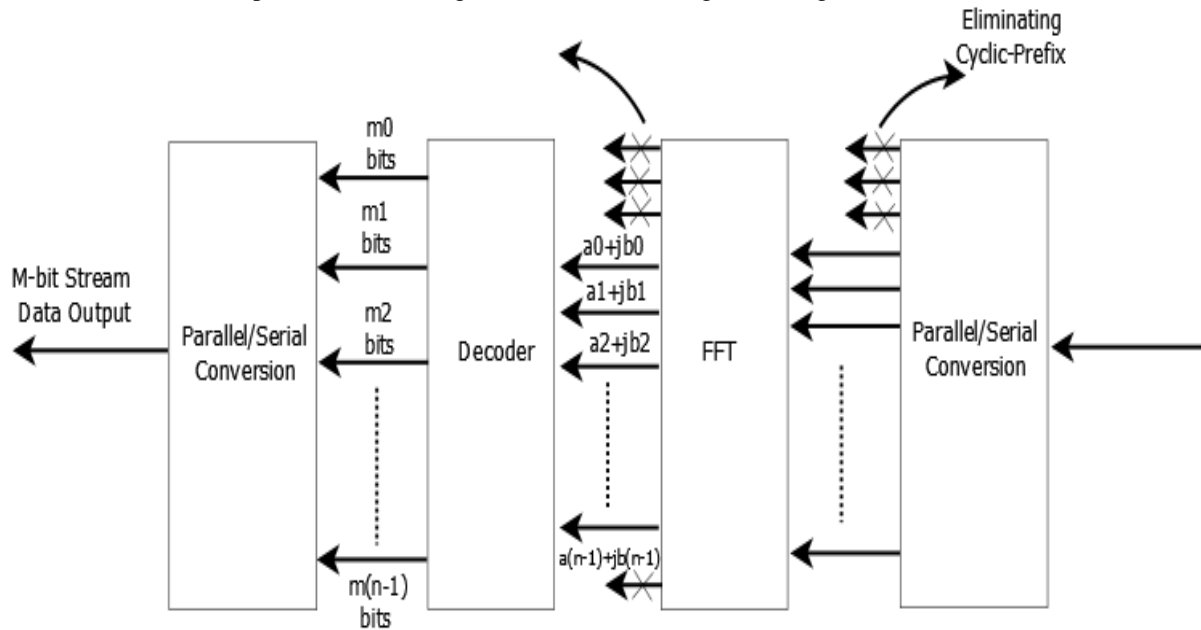


Fig.5. Receiver Part

**Serial to Parallel Conversion and vice versa**

Serial to parallel conversion is performed to convert the serial data to parallel data of required number. In this, the serial data is given as input to a shift register and (n-1) number of parallel data is taken as output simultaneously as a parallel data. The block diagram of the serial to parallel conversion is given in the Fig.6.

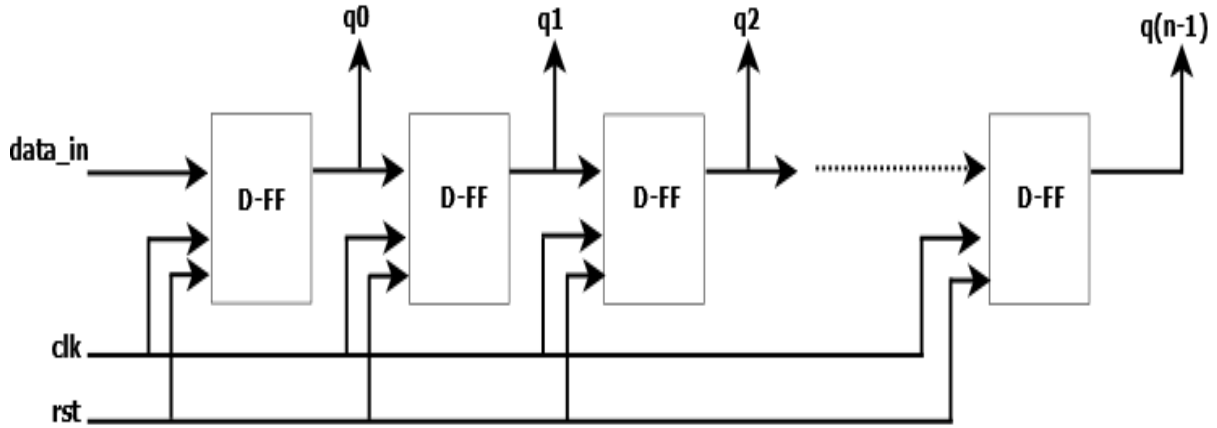


Fig.6. Serial to Parallel Conversion

Parallel to serial conversion is performed in order to convert the parallel data used for processing into serial data as output. Here, the (n-1) input are given to a n:1 Mux and the select lines are controlled through a counter for the selection of the parallel data and the output we get will be the serial data output. The block diagram of the parallel to serial conversion is given in the Fig.7.

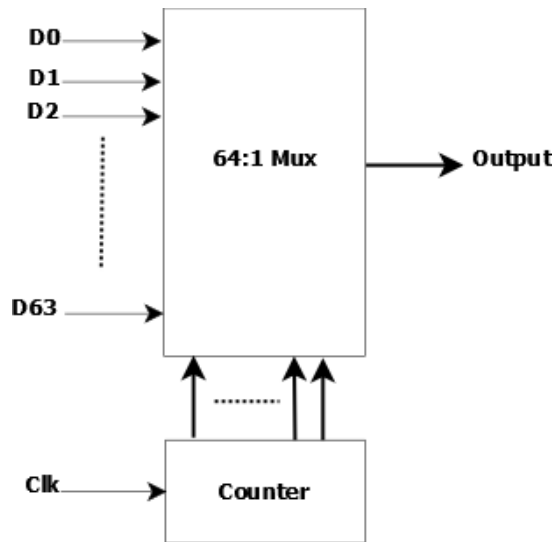


Fig.7. Parallel to Serial Conversion

**CORDIC Based FFT and IFFT**

The Fast Fourier Transform is one of the major concepts in signal processing. The signals in the time domain are converted into its respective frequency components. Here in this architecture, the 64 points are divided into 32, 16, 8, 4 and 2 points through 6 stages ( $2^6 = 64$ ), where, the 64 point time domain signals are divided into 64 time domain signals for the faster computation [12].

The equation of CORDIC is given as

$$\begin{aligned}
 x_{i+1} &= x_i - \sigma_i 2^{-i} y_i \\
 y_{i+1} &= y_i + \sigma_i 2^{-i} x_i \\
 \omega_{i+1} &= \omega_i - \sigma_i \alpha_i
 \end{aligned}$$

$$X(K) = \sum_{n=0}^{N-1} x(n) e^{-j \frac{2\pi Kn}{N}}$$

$$x(n) = \sum_{K=0}^{N-1} X(K) e^{j \frac{2\pi Kn}{N}}$$

We can rewrite FFT as

$$X(K) = \sum_{n=0}^{N-1} x(n) \cos\left(\frac{2\pi nk}{N}\right) + j \sum_{n=0}^{N-1} x(n) \sin\left(\frac{2\pi nk}{N}\right)$$

### Synchronizer

Due to the algorithm and hardware complexity it is possible in many cases that the synchronization between transmitter and receiver is not proper. For such case we need to use synchronization block for proper data synchronization. This block mainly consists of a small amount of memory with a corresponding controller. This synchronizer stores one data frame at a time into the memory block with the help of the controller unit. This data is used to reconstruct the whole frame. Until the reconstruction of a frame is not completed the next frame is not stored into the memory. The pseudo-code is given as:

Pseudo Code:

```

if(reset = ' 1')then
  address = ' 0';
  wen = ' 0';
  memready = ' 0';
else if(positive edge clock)then
  case(state ) is
  when s0 =>
  wen = ' 0'; memready = ' 0';
  address = address;
  when s1 =>
  wen = ' 1';
  if(memblock = ' 1')then
  address = ' 0';
  else
  address = 64;
  end if;
  when s2 =>
  address = address + 1;
  when s3 =>
  address = address + 1;
  numready = ' 1';
  end case;
end if;
if(reset = ' 1') then
  st = s0;
else if(positive edge clock) then
  case(state) is
  when s0 =>
  if(outputenable = ' 1') then
  st = s1;

```



```

end if;
when s1 => st = s0;
when s2 =>
if(address(5 downto 0) = 61) then
st = s3; end if;
when s3 => st = s0;
end case;
end if;

```

### Decoder

The pseudo-code for decoder implementation is given in Algorithm-1. The main purpose of the decoder is to recover the data using reverse constellation format. In our case we consider 4-point constellation.

#### Pseudo Code

```

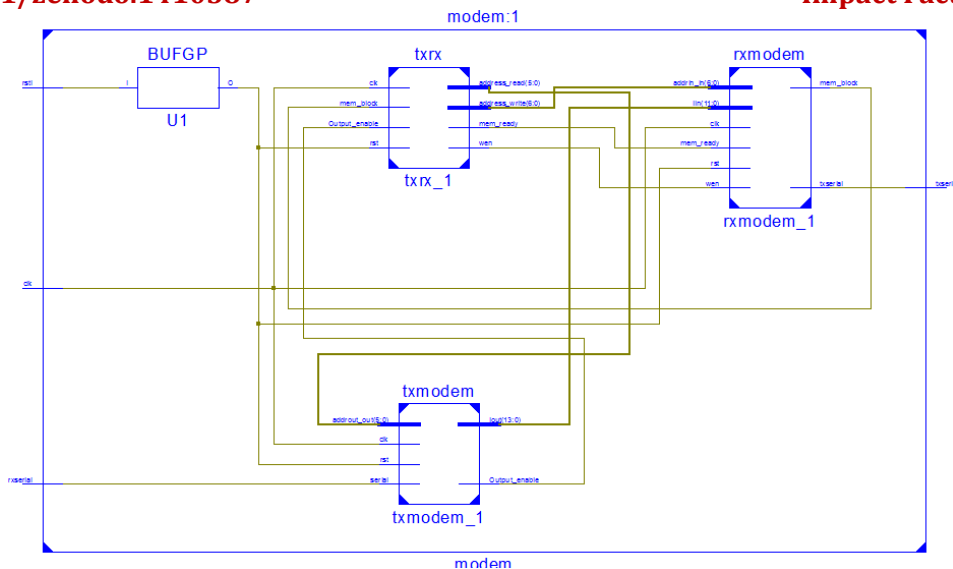
if(reset = '1')then
addresss = initialaddress;
txserial = '1';
elseif(positiveedgeclock)then
case(state)is
whens0 => txserial = '1';
address = initialaddress
whens1 ors2 ors3 ors3 => txserial => Ioutinserailformat
whens5 ors6 ors7 => txserial => Qoutinserailfashion
whens7 => txserial => Qoutinserialfashion
if(address! = max(address))then
incrementaddressvalue
else
addressvalueisinitial;
endif;
endcase;
endif;

```

## V. RESULTS

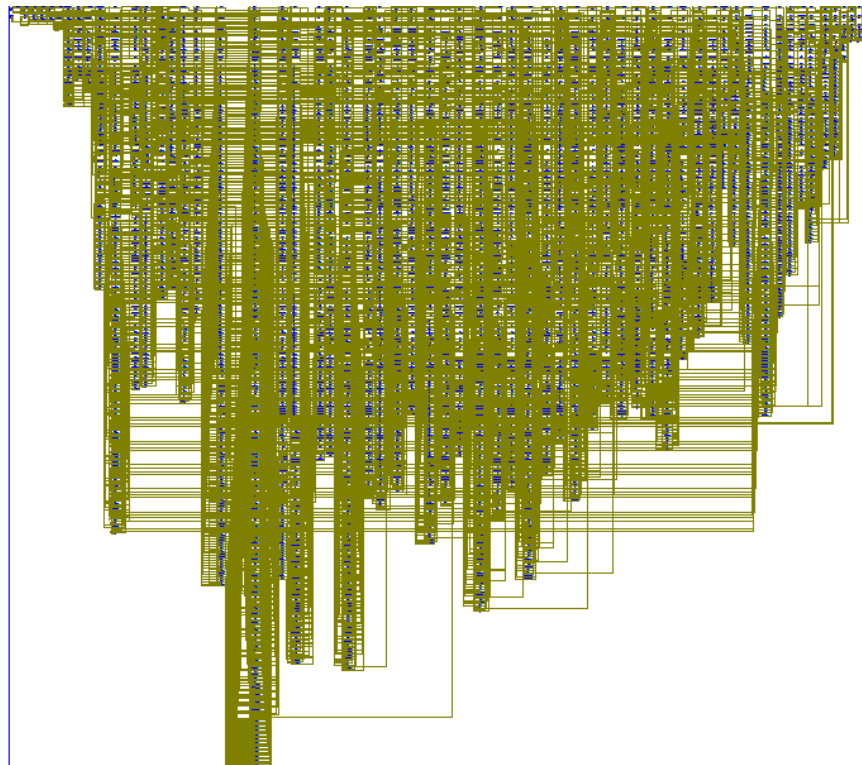
### FPGA Implementation

The proposed AOFDM architecture is implemented on Spartan-3 FPGA using Xilinx 14.5 tool. The synthesized schematic is given in Fig. 8 which indicates the top view connections and the technology synthesized schematic which indicates the mapping to specific library function is shown in Fig. 9.



**Fig.8. RTL Schematic**

But in FPGA any logic is implemented by mapping those logics into Look-Up-Tables (LUTs) [13]. The technology schematic will give the LUT level block diagram of the proposed architecture.



**Fig.9. Technology Schematic**

**Hardware Utilizations**

The hardware utilization of the proposed architecture including separately transmitter and receiver is given in Table 1. It is observed that the speed of the system is reduced to 125.97 MHZ compared to individual speed of transmitter

and receiver of approximately 134 Mhz since the synchronizer block consumes small delay for proper synchronization.

**Table 1: Hardware Utilizations**

Logic Utilization	Transmitter	Receiver	Total
Number of Slices	552	527	1098
Number of Slice Flip Flops	845	820	1684
Number of 4 input LUTs	994	935	1939
Number of BRAMs	5	5	10
Maximum Frequency (MHz)	134.571	134.120	125.976

## VI. COMPARISONS

The hardware resources utilizations of the proposed techniques are compared with the existing techniques presented by Naveen Kumar et al., [14] and Khaled Sobaihi et al., [15]. In both cases the proposed architecture uses less hardware resources than existing. The main reason is the uses of basic logic elements to construct the total architecture and the logical architectures are simplified at each block levels which reduced the overall hardware requirements.

**Table 2: Hardware Comparisons**

Parameters	Naveen Kumar et al., [14]	KhaledSobaihi et al., [15]	Proposed
Board	Virtex-4	Virtex-4	Spartan-3
Slice Registers	1428	2393	1098
Slice-FF	1149	3359	1684
4-input LUTs	2259	----	1939

## VII. CONCLUSIONS

In this paper, efficient VLSI architecture for AOFDM system to make low area communication systems is proposed.. The architecture of both transmitter and receiver are simulated using VHDL language and implemented on Spartan board. the implementation of Advanced OFDM involved 64-bits FFT/IFFT with 4-point QAM which are the minimal requirements of any real time multiplexed communication systems. In receiver side the encoded signal is needed to synchronize with receiver frequency, which is performed by synchronizer. To reduce hardware utilizations, each sub-module are redesigned using basic logic elements. The comparison results validates that the hardware utilization of proposed technique uses less hardware resources than existing.

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